# Formation of buried cavities in a monocrystalline semiconductor wafer

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Cited Documents: US4993143; US4579621

## Abstract

The method allows formation of buried cavities in a wafer (25) of monocrystalline semiconductor material. Initially, at least one cavity (21) is formed in a substrate (10) of monocrystalline semiconductor material, by timed TMAH etching silicon, then the cavity is covered with a material inhibiting epitaxial growth (22); finally, a monocrystalline epitaxial layer (26) is grown above the substrate (10) and the cavities (21). Thereby, the cavity (21) is completely surrounded by monocrystalline material. Starting from this wafer, it is possible to form a thin membrane (52). The original wafer (25) must have a plurality of elongate cavities or channels (21), parallel and adjacent to one another. Trenches (44) are then excavated in the epitaxial layer (26), as far as the channels (21), and the dividers between the channels are removed by timed TMAH etching.

# Description

[0001] The present invention relates to a method for forming horizontal buried channels or cavities in wafers of monocrystalline semiconductor material.

[0002] As known, at present, in many applications it is necessary to form cavities inside a monocrystalline silicon substrate, for example to obtain suspended masses of microactuators and/or sensors of various types, such as speed, acceleration and pressure sensors, or to isolate electronic components.

[0003] Now, buried cavities can be formed substantially in two ways. According to a first solution, shown in figure 1, two monocrystalline silicon wafers 1, suitably excavated and presenting each a half-cavity, are bonded to one another, using an adhesive layer (for example silicon oxide 2), so that the two half-cavities form a buried cavity 3.

[0004] According to a second solution, shown in figure 2, a monocrystalline silicon wafer 1, suitably excavated and comprising final cavities 4, is bonded to a glass layer 5 (anodic bonding process).

[0005] These solutions are costly, have a high criticality and low productivity, and are not fully compatible with the usual technological steps of microelectronics processing. In addition, the buried cavities or channels can be arranged only on a single plane, represented by line 7 in figure 3, and it is not possible to form cavities or channels at different heights, as shown in figure 4.

[0006] The object of the invention is thus to provide a method overcoming the disadvantages of the known solutions.

[0007] According to the present invention, there are provided a method for forming buried cavities in wafers of monocrystalline semiconductor material, and a wafer of monocrystalline semiconductor material, as defined respectively in claims 1 and 17.

[0008] To help understanding of the present invention, preferred embodiments are now described, purely by way of non-limiting example, with reference to the attached drawings, wherein:

figure 1 shows a cross-section of a semiconductor material wafer, formed according to a known solution;
figure 2 shows a cross-section of another known solution;
figure 3 shows an example of cavities formed according to the known methods;
figure 4 shows an example of cavities arranged on different levels;
figure 5 shows a plan view of a semiconductor material wafer, wherein the cavities have a first orientation with respect to the wafer;
figures 6-12 illustrate cross-sections of the wafer of figure 5, on an enlarged scale and in successive manufacture steps, according to a first embodiment;
figure 13 shows a plan view of a semiconductor material wafer, wherein the cavities have a second orientation with respect to the wafer;
figures 14 and 15 illustrate cross-sections of the wafer of figure 13, on an enlarged scale and in successive manufacture steps, according to a second embodiment;
figure 16 illustrates a cross-section of the wafer of figure 13, on an enlarged scale and in a manufacture step according to a third embodiment;
figures 17-19 show cross-sections of silicon wafers, provided with cavities with different shapes and positions;
figures 20 and 21 show perspective cross-sections of a wafer in two successive steps, for forming thin membranes;
figures 22-26 show cross-sections of the wafer of figure 21, taken along plane XXII-XXII of figure 21, in successive steps; and
figures 27-28 show cross-sections of the wafer of figure 21, taken along a plane parallel to plane XXII-XXII, in subsequent steps with respect to figures 22-26.

[0009] Figure 5 shows a monocrystalline silicon wafer 10, wherein a cavity or channel is to be formed, extending at 45 DEG with respect to the flat part of the wafer, determined by orientation &lang&110&rang&.

The surface of wafer 10 has orientation &lang&100&rang&.

[0010] As shown in figure 6, initially a first oxide layer is grown on surface 11 of wafer 10; the first oxide layer having a thickness comprised, for example, between 20 and 60 nm; then a nitride layer is deposited, having a thickness between 90 and 150 nm. Using a resist mask, the uncovered portions of the first nitride layer and of the first oxide layer are dry etched, and the resist mask is then removed; thereby, the portions of the first oxide layer and of the first nitride layer, remaining after the dry etching (oxide portions 12 and nitride portions 13) form a hard mask, indicated at 14.

[0011] Subsequently, using the hard mask 14, the wafer 10 is etched (first trench etching), forming first trenches 15 (figure 6), having a width, for example, between 1 and 3 mu m (and preferably 2 mu m), and a depth depending on the structures to be formed, for example of a few microns.

[0012] Subsequently, as shown in figure 7, the wafer 10 is subjected oxidation, thus forming a second oxide layer 18 having a thickness, for example, comprised between 20 and 60 nm, covering the walls and base of the first trenches 15, and connected to the oxide portions 12, such as to form a single layer. Then a second nitride layer 19 is deposited, having a thickness, for example, comprised between 90 and 150 nm, and connected to the nitride portions 13, to form a single layer.

[0013] Subsequently, figure 8, the nitride material is dry etched and the oxide material is dry or wet etched. This etching causes removal of the horizontal portions of the nitride layer 19 and oxide layer 18 on the bottom of the first trenches 15, and of the horizontal portions of the nitride layer 19, above surface 11 of wafer 10, thus forming a first protective coating or spacer 20 on the walls of the first trenches 15, and exposing the monocrystalline silicon on the bottom of the first trenches 15. The hard mask 14 also remains on surface 11 of wafer 10.

[0014] Then, figure 9, the silicon material below the first trenches 15 is time etched using TMAH (tetramethylammoniumhydroxide). This etching, of anisotropic type, generates cavities 21, having a width d (at the widest point) of, for example, 10-100 mu m, and therefore much larger than the first trenches 15. If the first trenches 15 have an elongate shape, in a direction perpendicular to the drawing plane, the cavities 21 form elongate channels.

[0015] Subsequently, figure 10, the walls of cavities 21 are covered with an inhibiting layer 22, which does not allow epitaxial growth. To this end, for example, a rapid oxidation step can be carried out, to grow an oxide layer (with a greater thickness than the oxide portions 12 and 18, covering the surface 11 of wafer 10 and the wall of the first trench 15, as described hereinafter, for example comprised between 60 and 100 nm), or a layer selected among deposited oxide, nitride, or TEOS-tetraethylorthosilicate, may be deposited.

[0016] Then, figure 11, the first spacers 20 are removed from the walls of the first trenches 15, and the hard mask 14 is removed from the surface 11 of the wafer 10. During removal of the oxide portions 12 and 18, part of the inhibiting layer 22 is also removed; the inhibiting layer 22, is not removed completely since it is thicker, as already stated, and remains to an extent sufficient to ensure complete covering of the walls of the cavities 21.

[0017] Subsequently, figure 12, epitaxial growth is carried out, using as a nucleus the monocrystalline silicon of wafer 10; consequently, monocrystalline silicon is grown horizontally, inside the first trenches 15, thus closing the latter, and vertically, from the surface 11 (which can no longer be seen in figure 12). On the other hand, the silicon is not grown inside the cavities 21, due to the presence of the inhibiting layer 22. Thus a monolithic wafer 25 of monocrystalline silicon is obtained, formed by substrate 10 and an epitaxial layer 26, and accommodating closed cavities 21, delimited internally by the inhibiting layer 22.

[0018] If the trenches 15 (and thus the cavities 21) are oriented at 0 DEG and 90 DEG with respect to the flat part of the wafer 10 (as shown in plan view in figure 13), after forming the first spacers 20 (figure 8), and before TMAH etching (figure 9), a second trench etching is carried out, masked by the hard mask 14 and the first spacers 20 (figure 14). Thereby a deep trench 30 is formed, the lower portion 30a whereof extends below the first spacers 20.

[0019] Subsequently, figure 15, timed TMAH etching is carried out, forming a cavity 21' around the lower part 30a of the deep trenches 30 (shown by broken line in figure 15). Subsequently, the process already

described with reference to figures 11, 12 is carried out, forming an inhibiting layer 22, removing the hard mask 14 and the first spacers 20, and growing an epitaxial layer, to obtain the final structure of figure 12.

[0020] According to a different embodiment, again with trenches 15 oriented at 90 DEG with respect to the flat part 110 of the wafer 10 (as shown in figure 13), after forming the hard mask 14 and first trench etching, forming the first trenches 15 (figure 6), timed TMAH etching is carried out directly, forming a cavity 21" around the first trenches 15, figure 16. Similarly to the above described case, then the steps of forming an inhibiting layer 22, removing the hard mask 14 and the first spacers 20, and epitaxial growth are carried out.

[0021] The wafer 25 thus obtained may integrate electronic components and/or integrated microstructures in the epitaxial area above the cavities 21, 21', 21", in a known manner.

[0022] According to the orientation of cavities 21, 21', 21", the duration of TMAH etching, the number and arrangement of the cavities 21, 21', 21", it is possible to obtain various geometries, as shown in figures 17-19, wherein, for simplicity, the inhibiting layer has been omitted. In detail, figure 17 shows a wafer 25 accommodating a plurality of cavities 21 with a substantially octagonal shape, arranged parallel to one another, in a direction at right-angle with respect to the drawing plane and at a same height. The wafer 25 in figure 17 is obtained in the above-described manner, and selecting a TMAH etching time that does not allow complete silicon etching.

[0023] Figure 18 shows a wafer 25 accommodating a plurality of cavities 36 square-shaped (rotated by 45 DEG ) or rhombus-shaped, arranged similarly to the previous case parallel to one another, at a right-angle with respect to the drawing plane, at a same height. The wafer 25 in figure 18 is obtained furthering the TMAH etching, until obtaining the final geometry (square or rhombus, depending on the orientation of the cavities 36 with respect to the crystallographic plane of the wafer 25) caused by the TMAH etching.

[0024] Figure 19 shows a wafer 25 accommodating a plurality of cavities 38, 39, having an octagonal shape and arranged at different heights in wafer 25. The wafer 25 of figure 19 is obtained by forming first trenches 15 with different depths (with different etching times), or different widths (such that the final depth of the channels 38, 39 is different); or repeating the process described with reference to figures 6-12 or 14-15 or 16 several times, forming one or more cavities 39 at a first height, carrying out first epitaxial growth, forming one or more cavities 38 at a greater height, carrying out second epitaxial growth, and so on.

[0025] The above-described method may be also used to form monocrystalline silicon membranes with a reduced thickness (for example between 1 and 3 mu m, if the membrane is used as a sensor, and approximately 10 mu m, if electronic components are to be integrated), above an air gap of desired shape, as described hereinafter with reference to figures 20-29.

[0026] To this end, beginning for example from wafer 25 of the type shown in figure 17, illustrated in perspective in figure 20, comprising a plurality of cavities or channels 21 having a length l (in direction y), much greater than their maximum width d (in direction x). In particular, the channels 21 have a length l linked to the desired length of the membrane, and are of such a number to extend along the entire width (in the direction x) of the membrane. In addition, the upper side of the channels 21 is arranged at a depth, from the surface of the wafer 25, equivalent to the desired thickness for the membrane.

[0027] As shown in figures 21 and 22, trench etching of silicon above the cavities 21 is then carried out, to form at least two connection trenches, extending parallel to one another, in a direction perpendicular to the length of the cavities 21 (parallel to the x axis in the example shown). For this purpose, in a known manner, a third oxide layer 40 is initially deposited or grown and a third nitride layer 41 is then deposited; the oxide layer 40 and the nitride layer 41 are photolithographically defined, to form a second hard mask 42 completely covering the wafer 25, except the parts where the connection trenches are to be formed; the exposed silicon is then etched, thus forming connection trenches 44, extending as far as the inhibiting layer 22 of cavities 21.

[0028] Subsequently, figure 23, the surface of the connection trenches 44 is oxidized, forming a fourth oxide layer 45 (which, above the cavities 21, is integral with the inhibiting layer 22), and a fourth nitride layer 46 is deposited.

[0029] Then, figure 24, the nitride and then the oxide material of layers 45, 46 is dry etched, thus removing

the latter from the horizontal portions above the second hard mask 42 and from the bottom of the connection trenches 44; thereby, spacers 47 are formed above the cavities 21 and on the walls of the trenches 22. In this step, part of the inhibiting layer 22 (if of oxide), present in the upper part of the cavities 21 is also removed, as also shown in figure 25, showing a cross-section of a connection trench 44 taken along a cross-section plane perpendicular to figure 24.

[0030] Subsequently, figure 26, the inhibiting layer 22 covering the walls of the cavities 21 is wet etched. The inhibiting layer 22 is thus completely removed. Subsequently, figure 27, the silicon material surrounding the cavities 21 is time etched, to completely remove the diaphragms (indicated at 50 in figure 26) separating the cavities 21 from each other. Thereby an air gap 51 is formed, extending continuously below a monocrystalline silicon portion forming a membrane 52, as can be seen in cross-section in figure 27, taken along a plane parallel to figure 26 and not intersecting a connection trench 44. In this step, planarization of the upper and lower walls of the gap 51 is also obtained, as can be seen in figure 27, wherein the original cavities 21 are shown in broken lines, to help understanding.

[0031] After the second hard mask 42 has been removed, a wafer 54 is thus obtained, as shown in figure 28, wherein the membrane 52 has a thickness to length ratio s/L <<1, for example, comprised between 0.1 and 0.01.

[0032] The advantages of the described method are apparent from the preceding description. In particular, it is emphasised that the method allows forming completely buried cavities and channels, using steps common in microelectronics, and thus reliably and repeatably. It also allows obtaining different geometries, depending on requirements, with an extensive variety of shapes. Additionally, membranes may be formed having the desired shapes and dimensions, depending on the necessary components (electronic or micro-electric-mechanical).

[0033] Finally, it is apparent that many modifications and variants can be made to the method described and illustrated here, all of which come within the scope of the invention, as defined in the attached claims.

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# Claims

1. A method for forming buried cavities in a wafer (25) of monocrystalline semiconductor material, comprising the step of forming at least one cavity (21; 21'; 21") in a substrate (10) of monocrystalline semiconductor material, characterised in that it comprises the step of growing a monocrystalline epitaxial layer (26) on said substrate (10) and said at least one cavity (21), thereby obtaining a wafer (25) of monocrystalline semiconductor material, containing at least one buried cavity (21) completely surrounded by said monocrystalline material.

2. A method according to claim 1, characterised in that before said step of growing an epitaxial layer (26), the step is carried out of covering walls of said cavity (21) with material inhibiting epitaxial growth (22).

3. A method according to claim 2, characterised in that said material inhibiting epitaxial growth comprises oxide.

4. A method according to claim 2, characterised in that said material inhibiting epitaxial growth comprises TEOS.

5. A method according to claim 2, characterised in that said material inhibiting epitaxial growth comprises nitride.

6. A method according to any one of the preceding claims, characterised in that said step of forming at least one cavity (21; 21') comprises the steps of:

forming at least one first trench (15) in said substrate (10);
covering lateral walls of said first trench (15) with first protective regions (20) of a material resistant to etching of said monocrystalline semiconductor material; and
anisotropically etching said substrate (10), below said first trench (15).

7. A method according to any one of claims 1-5, characterised in that said step of forming at least one cavity (21") comprises the steps of:

forming at least one first trench (15) in said substrate (10); and
anisotropically etching said substrate (10), to remove said semiconductor material around said first trench (15).

8. A method according to claim 6 or claim 7, characterised in that said anisotropic etching is TMAH etching.

9. A method according to any one of claims 6-8, characterised in that said anisotropic etching is timed etching.

10. A method according to claim 6, characterised in that before said step of anisotropically etching, the step is carried out of forming at least one second trench (30a) aligned with, and arranged below, said first trench (15).

11. A method for forming a membrane (52) of monocrystalline semiconductor material, arranged above an air gap (51), comprising the steps of:

forming a wafer (25) of monocrystalline semiconductor material according to any one of claims 1-10, with a plurality of cavities defining buried channels (21) adjacent and separated from each other by dividers (50);
forming third trenches (44) in said epitaxial layer (26), said third trenches extending transversely to said buried channels (21) from a surface of said wafer, as far as said buried channels; and
removing said dividers (50).

12. A method according to claim 11, characterised in that, after said step of forming third trenches (44), the step is carried out of forming second protective regions (47) extending on the walls of said third trenches.

13. A method according to claim 11 or claim 12, wherein said buried channels (21) have walls covered by a layer inhibiting epitaxial growth (22), characterised in that said step of removing said dividers (50) comprises the steps of:

removing said layer inhibiting epitaxial growth (22); and
anisotropically etching said semiconductor material.

14. A method according to claim 13, characterised in that said anisotropic etching comprises TMAH timed etching.

15. A wafer (25) of monocrystalline semiconductor material, characterised by at least one buried cavity (21) completely surrounded by said monocrystalline material.

16. A wafer according to claim 17, characterised in that said at least one buried cavity (21) is covered with a layer of material inhibiting epitaxial growth (22).

17. A wafer according to claim 16, characterised in that said material inhibiting epitaxial growth comprises oxide.

18. A wafer according to claim 16, characterised in that said material inhibiting epitaxial growth comprises TEOS.

19. A wafer according to claim 16, characterised in that said material inhibiting epitaxial growth comprises nitride.

20. A wafer according to any one of claims 15-19, characterised by a plurality of buried channels (21) adjacent and separated from each other by dividers (50).

21. A wafer according to any one of claims 15-20, characterised by a plurality of buried cavities (38, 39) at different heights.

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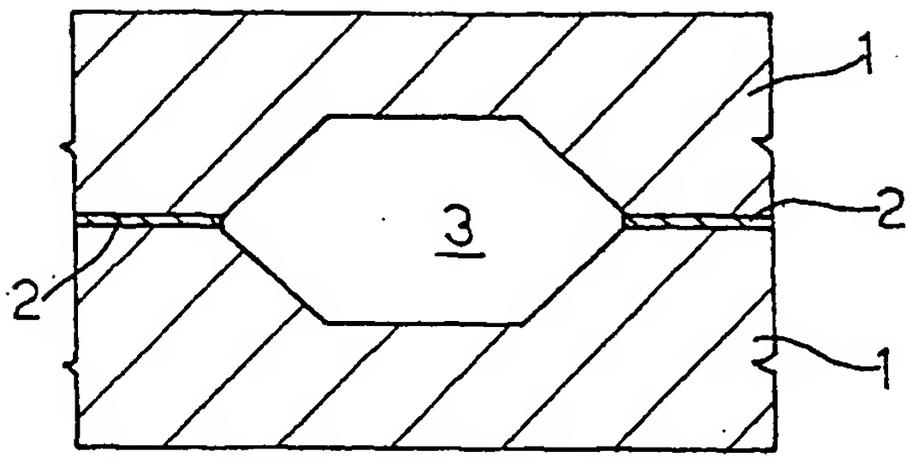


Fig. 1

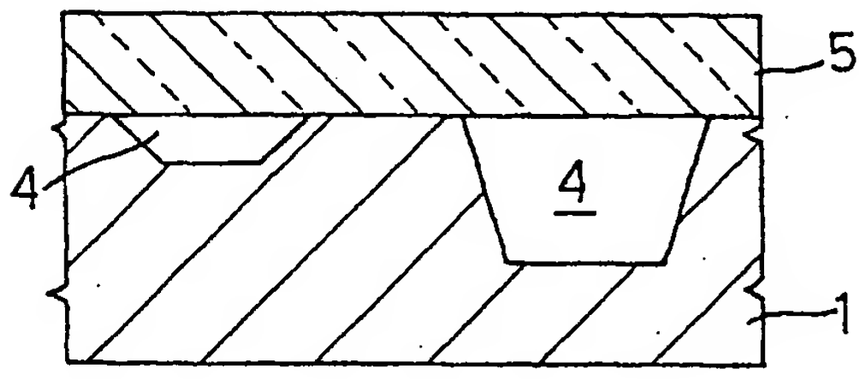


Fig. 2

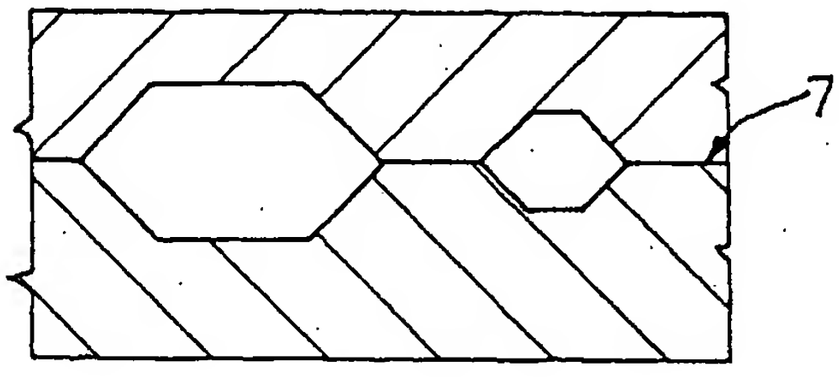


Fig. 3

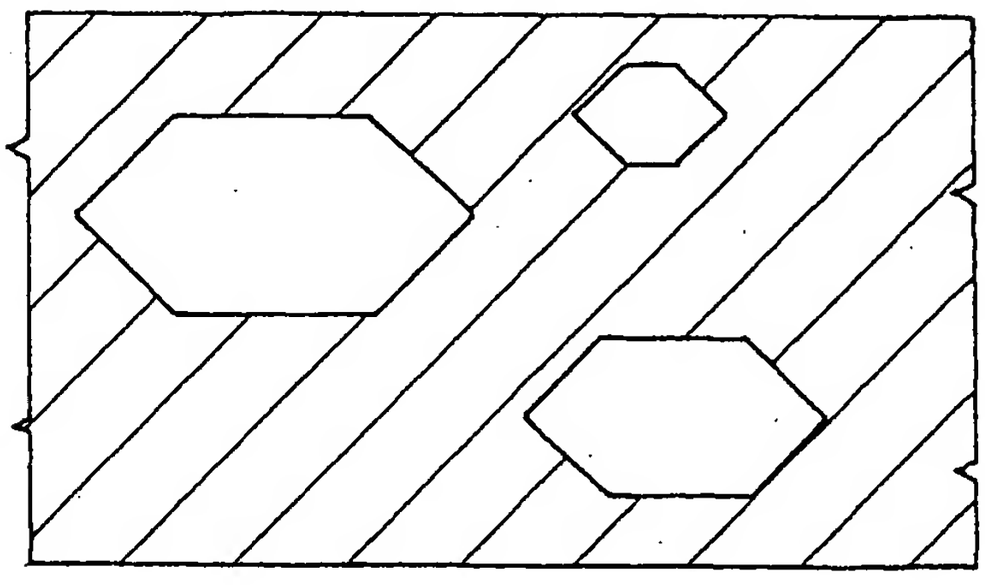

Fig. 4

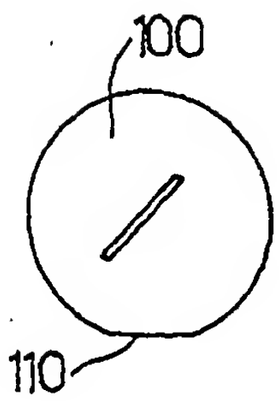


Fig.5

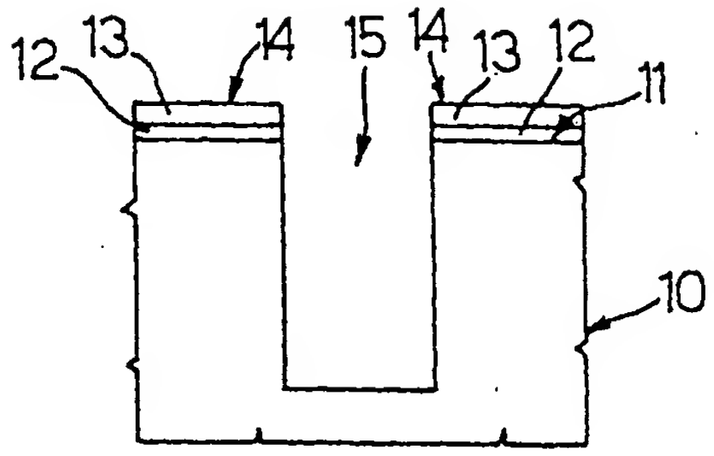


Fig.6

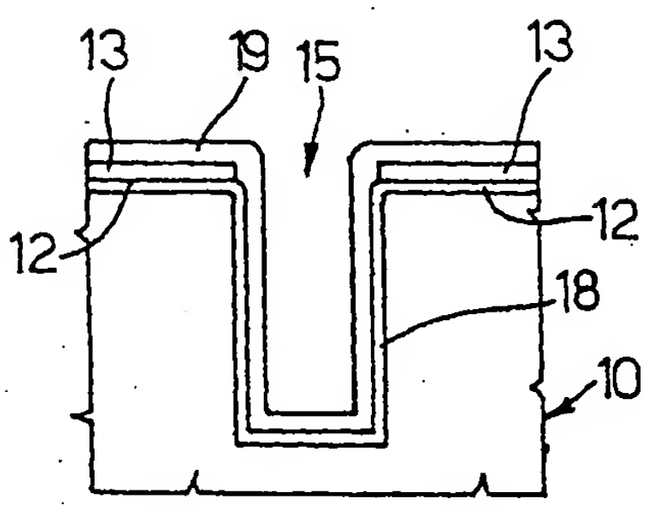


Fig.7

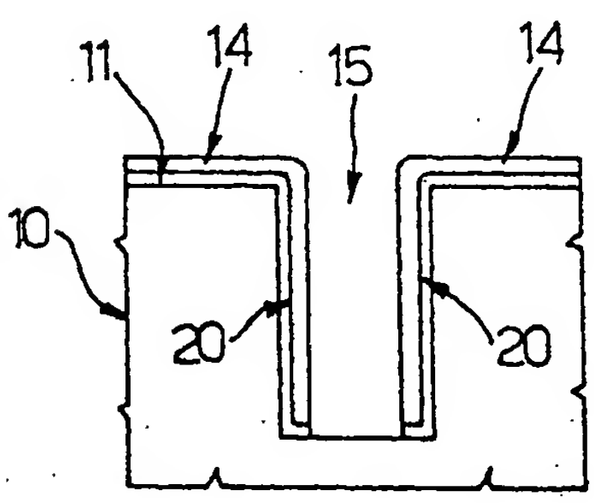


Fig.8

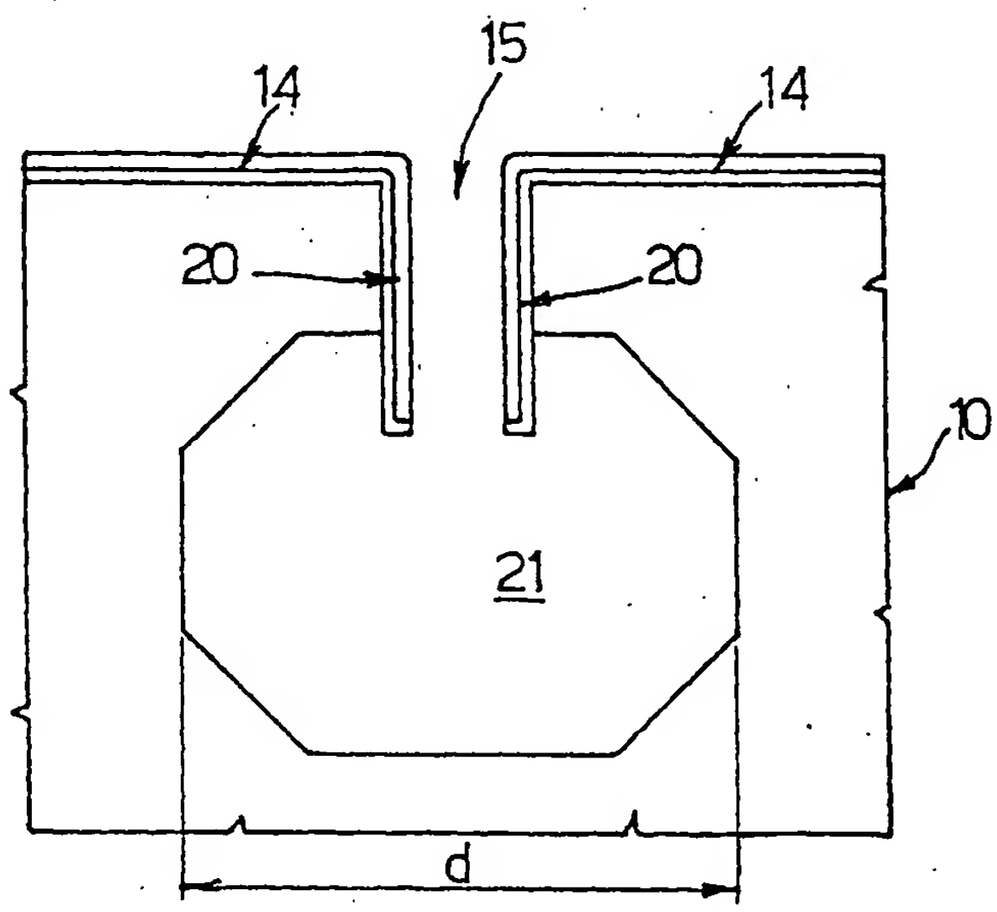


Fig.9

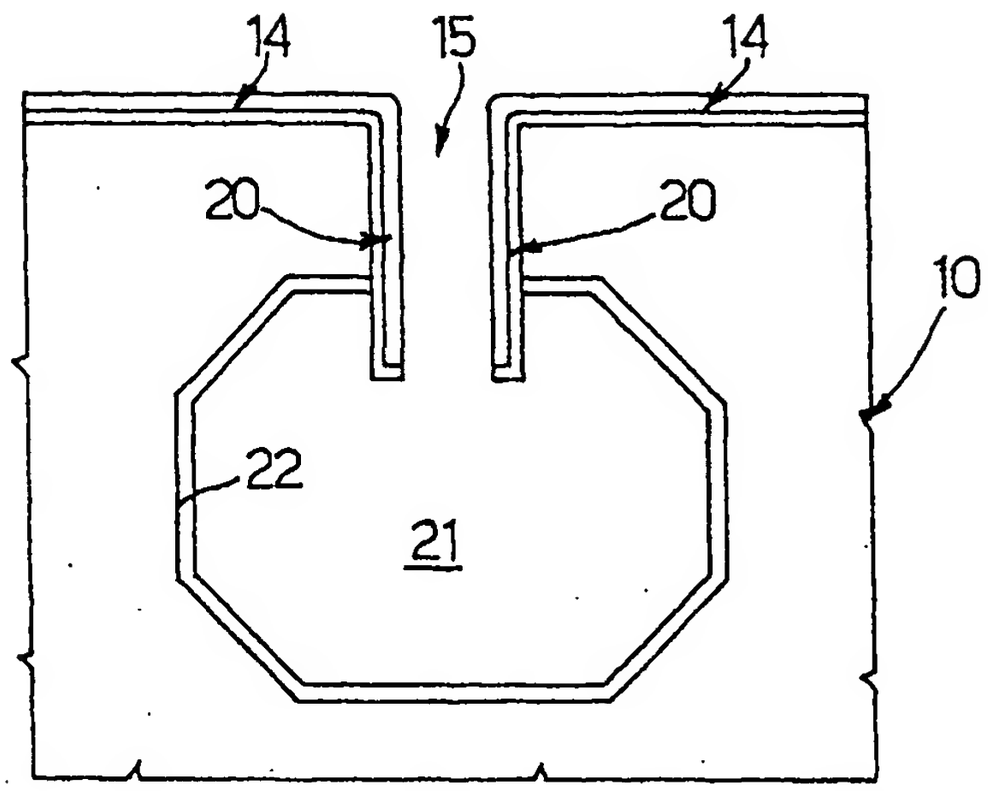


Fig.10

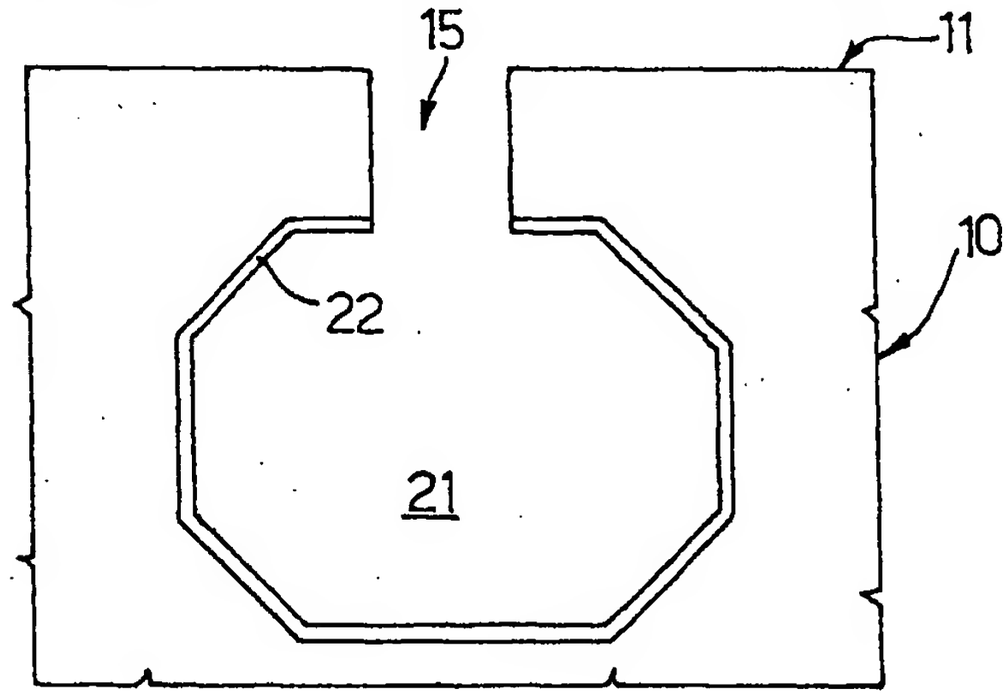


Fig.11

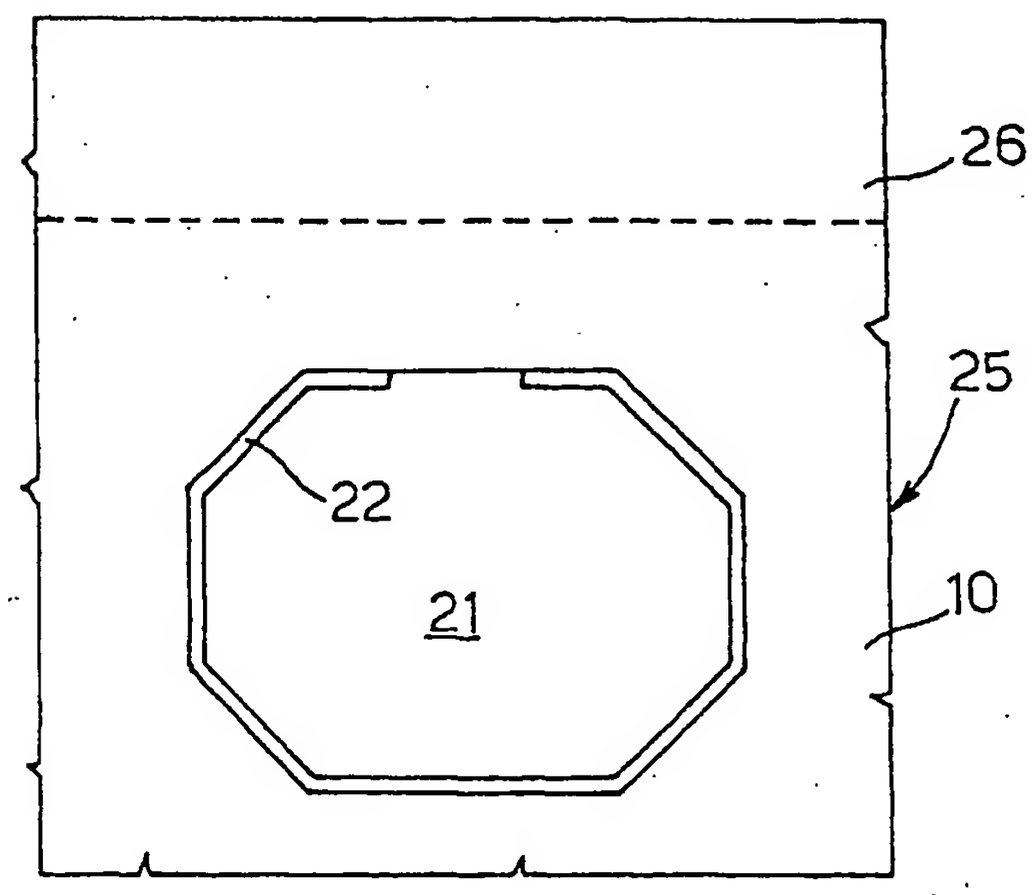


Fig.12

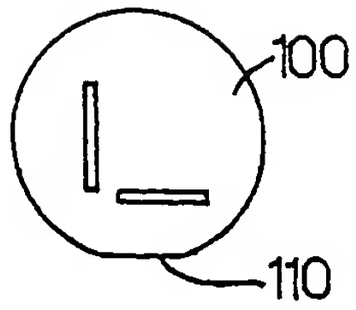


Fig.13

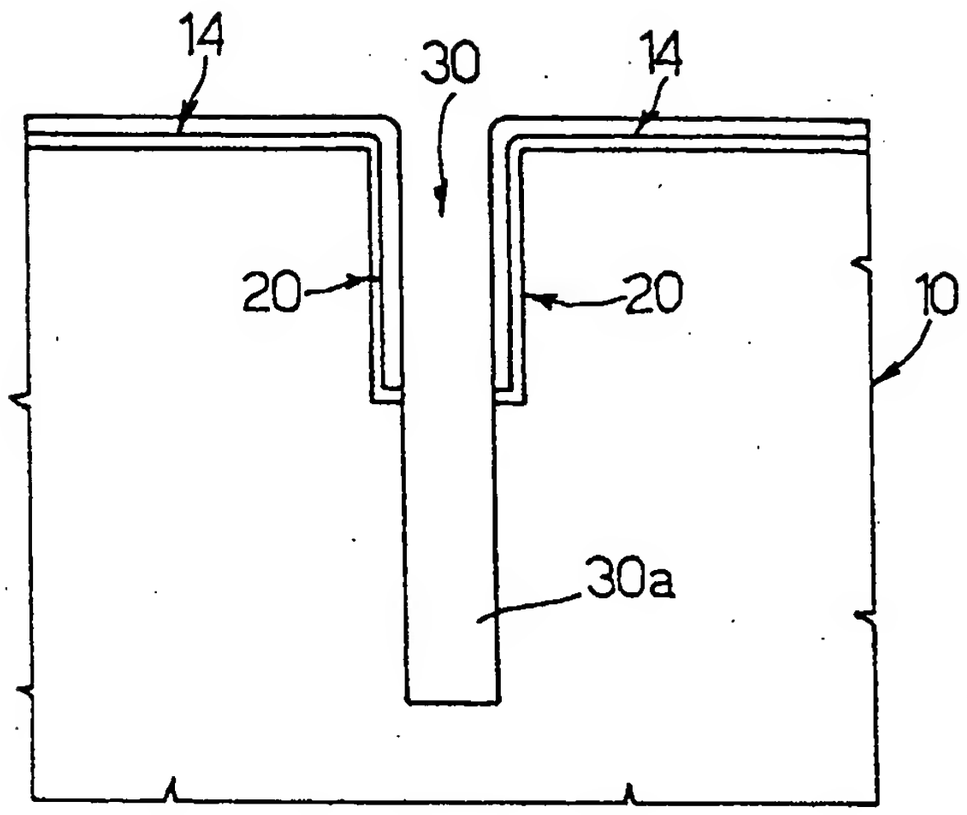


Fig.14

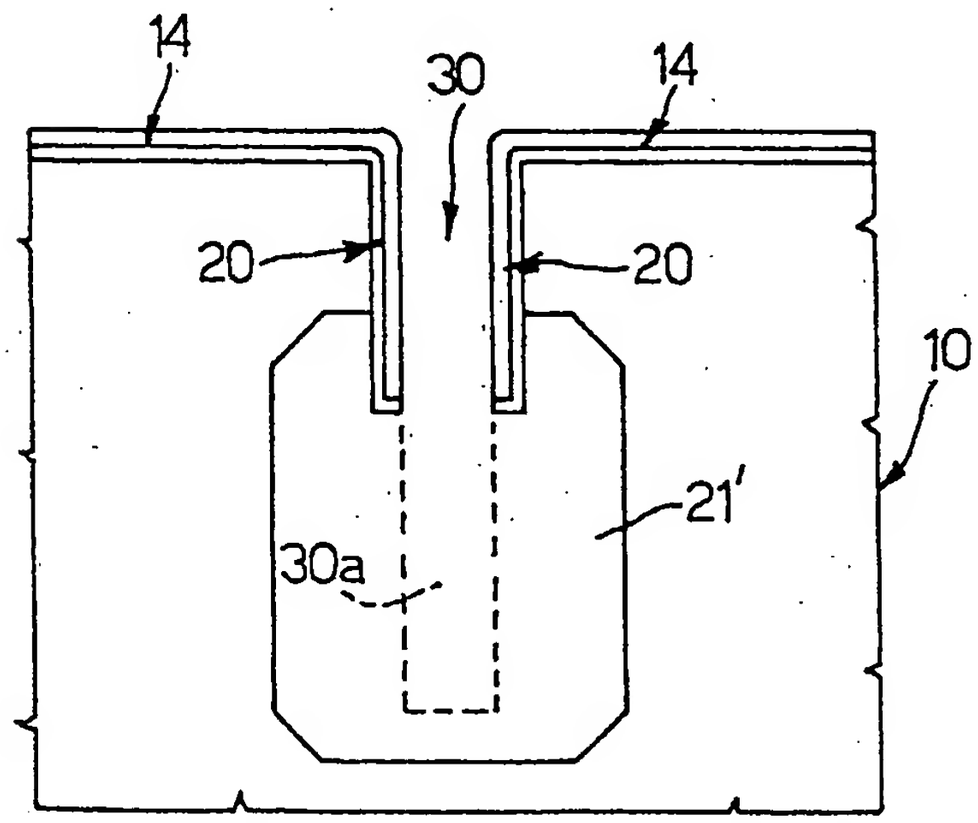


Fig.15

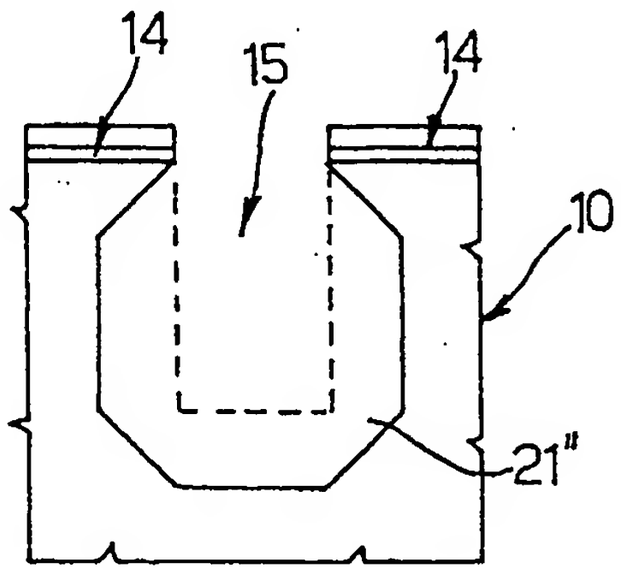


Fig.16

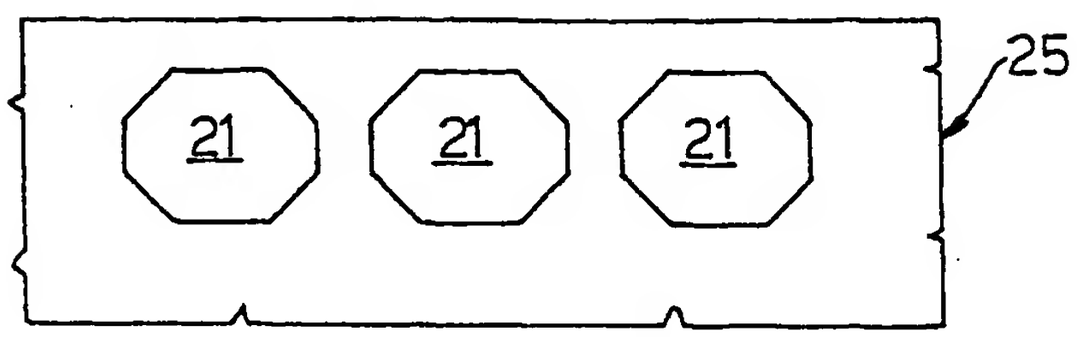


Fig. 17

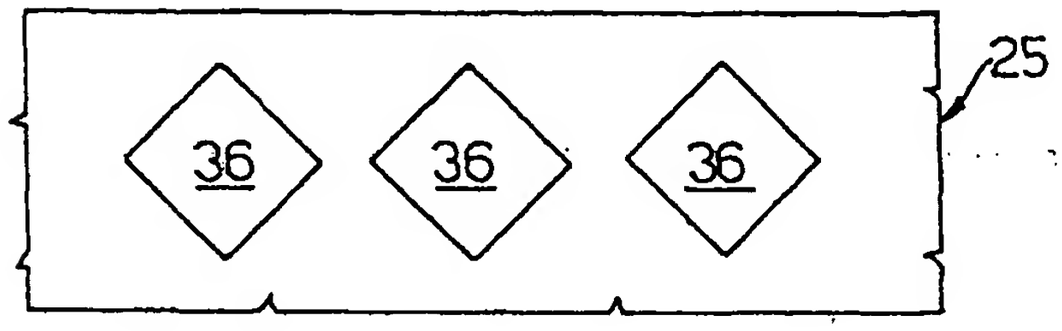


Fig. 18

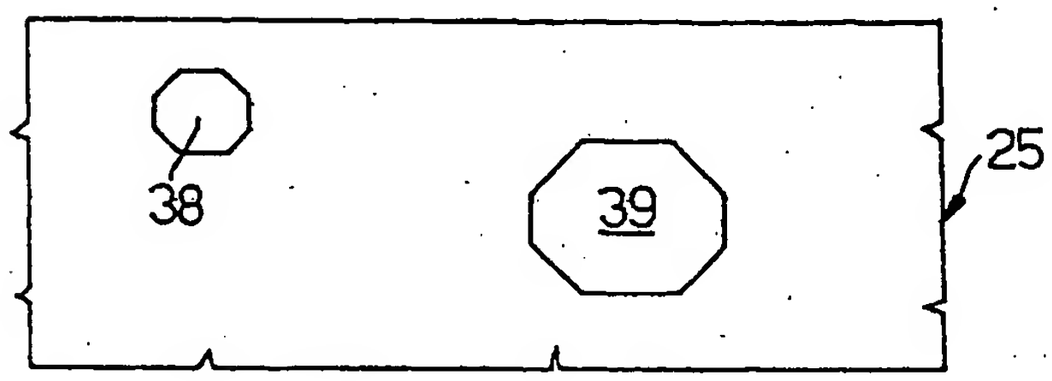


Fig. 19

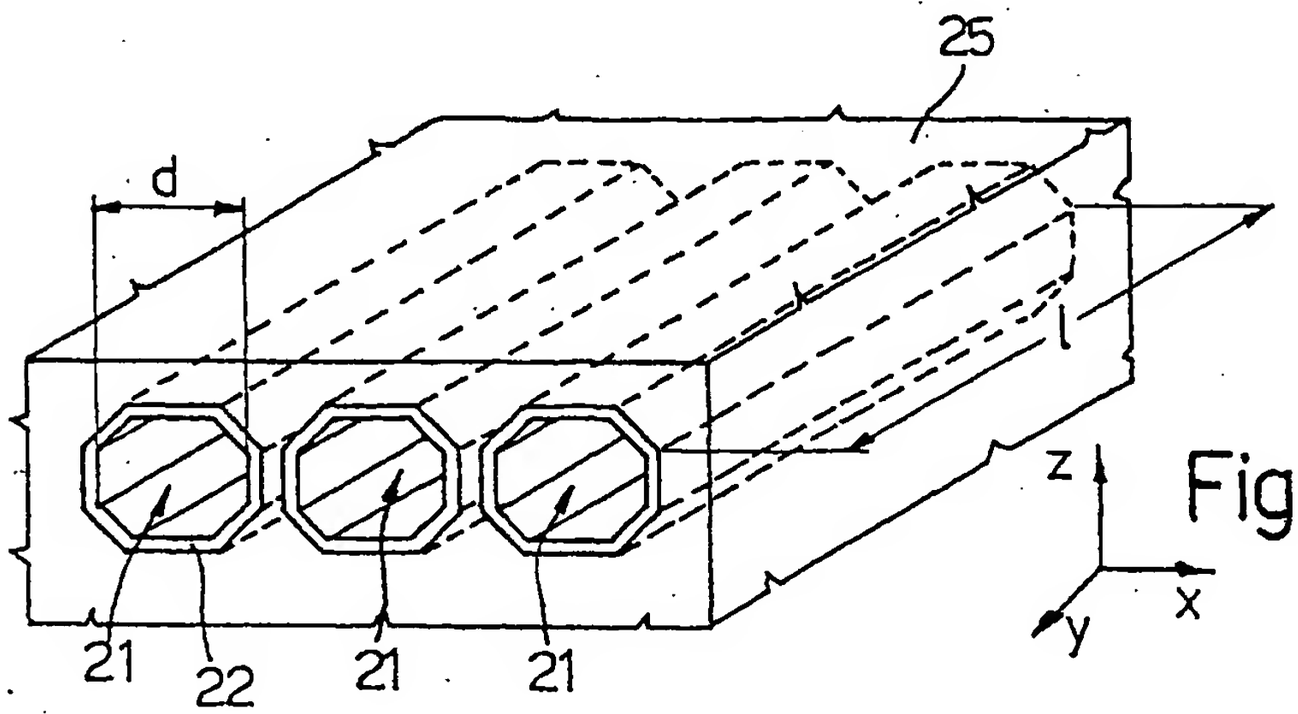


Fig. 20

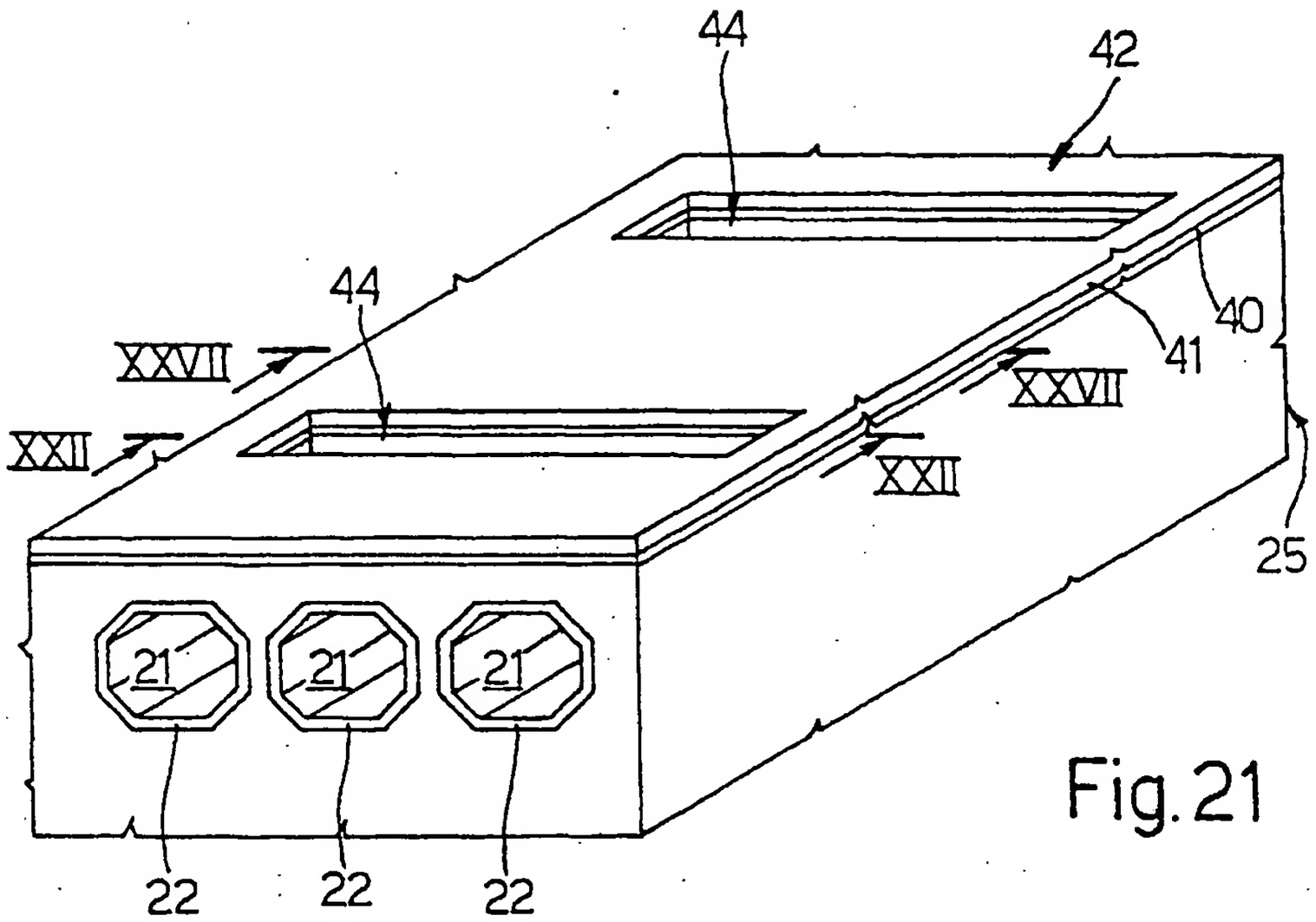


Fig.21

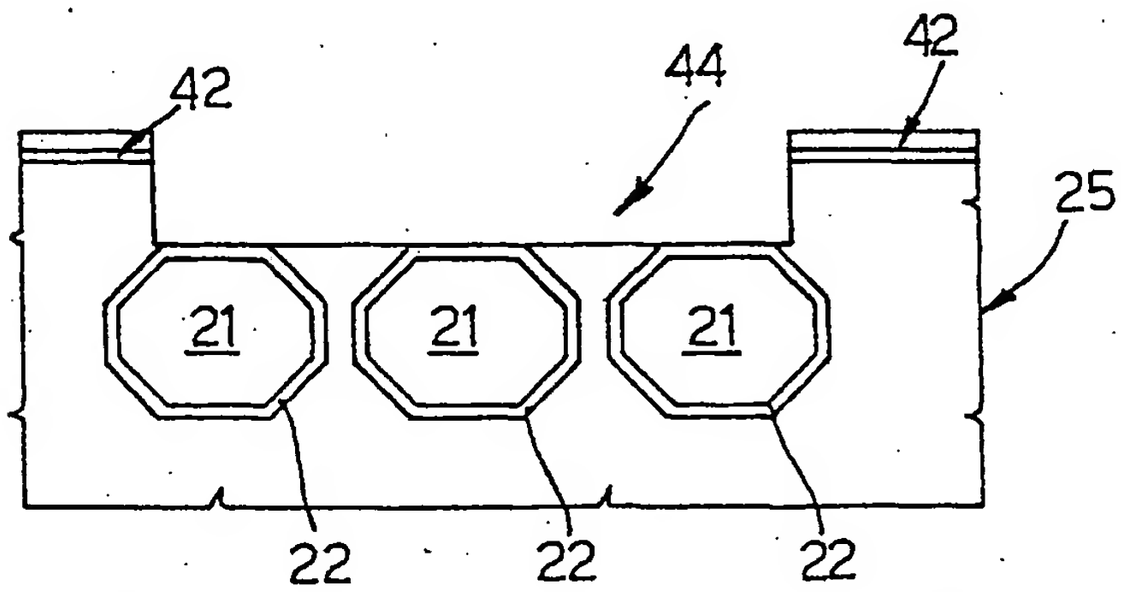


Fig.22

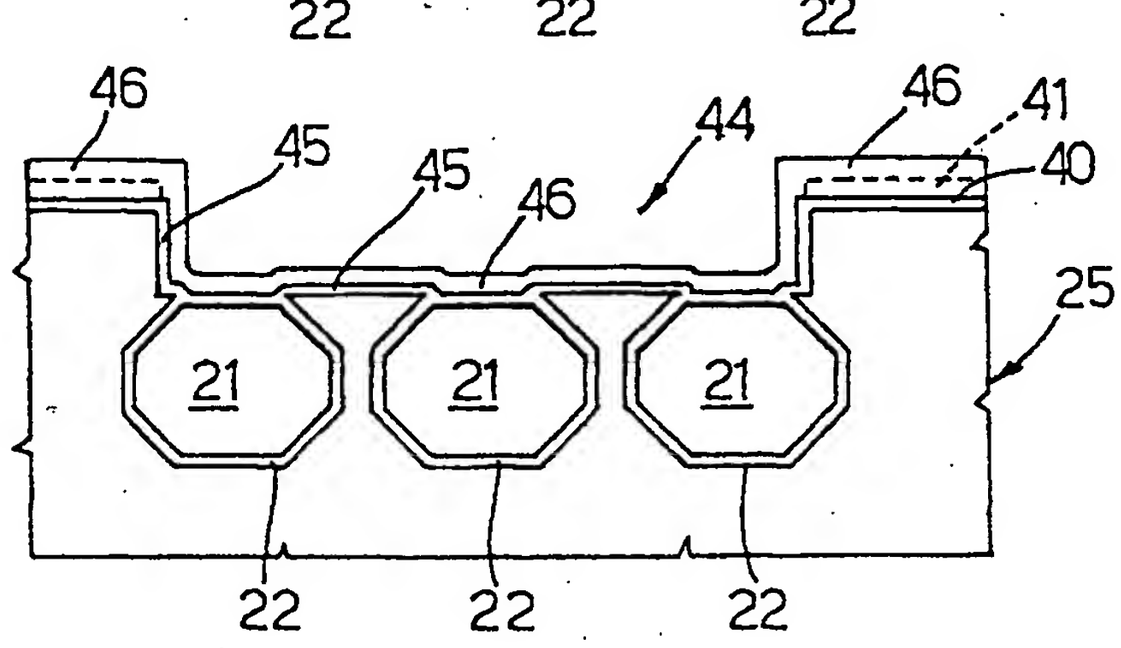


Fig. 23

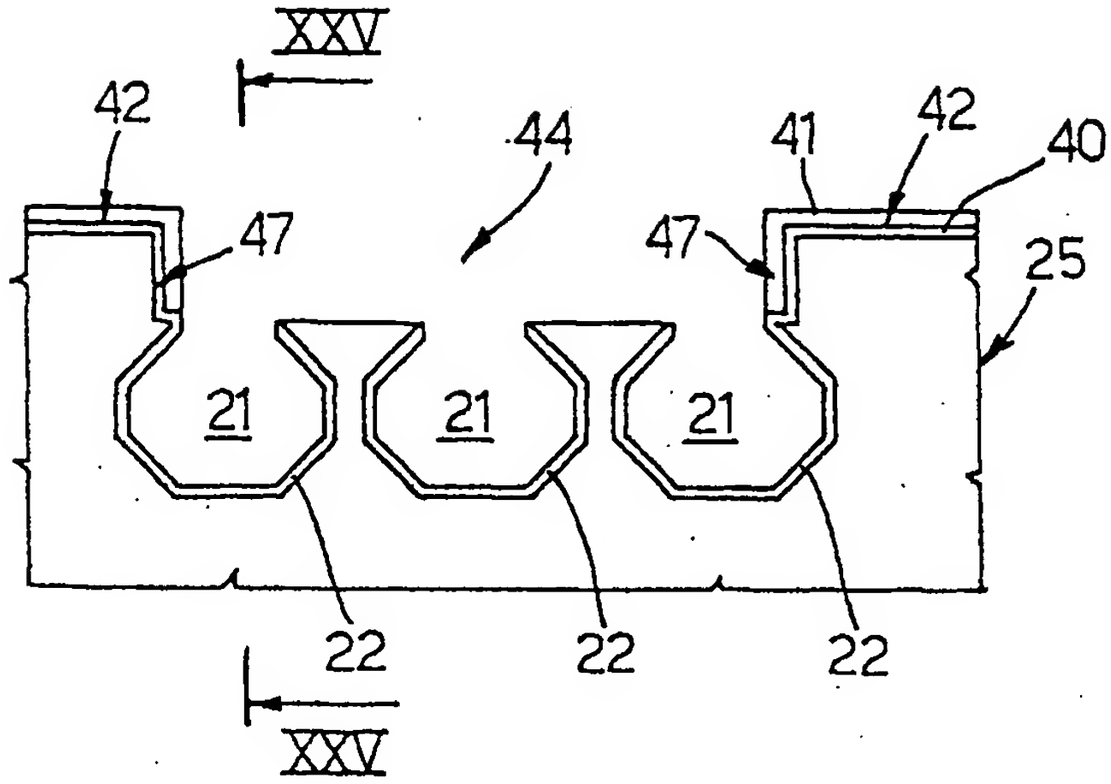


Fig. 24

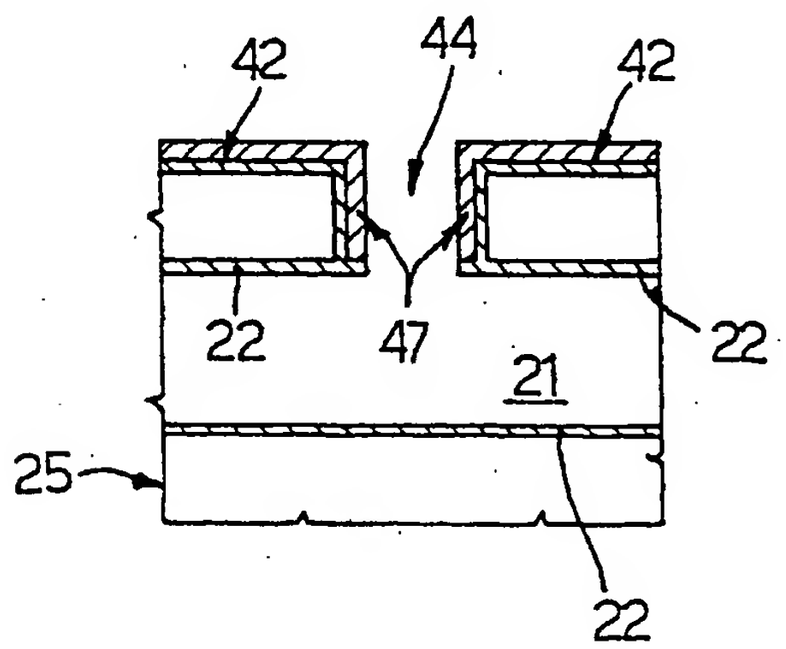


Fig. 25

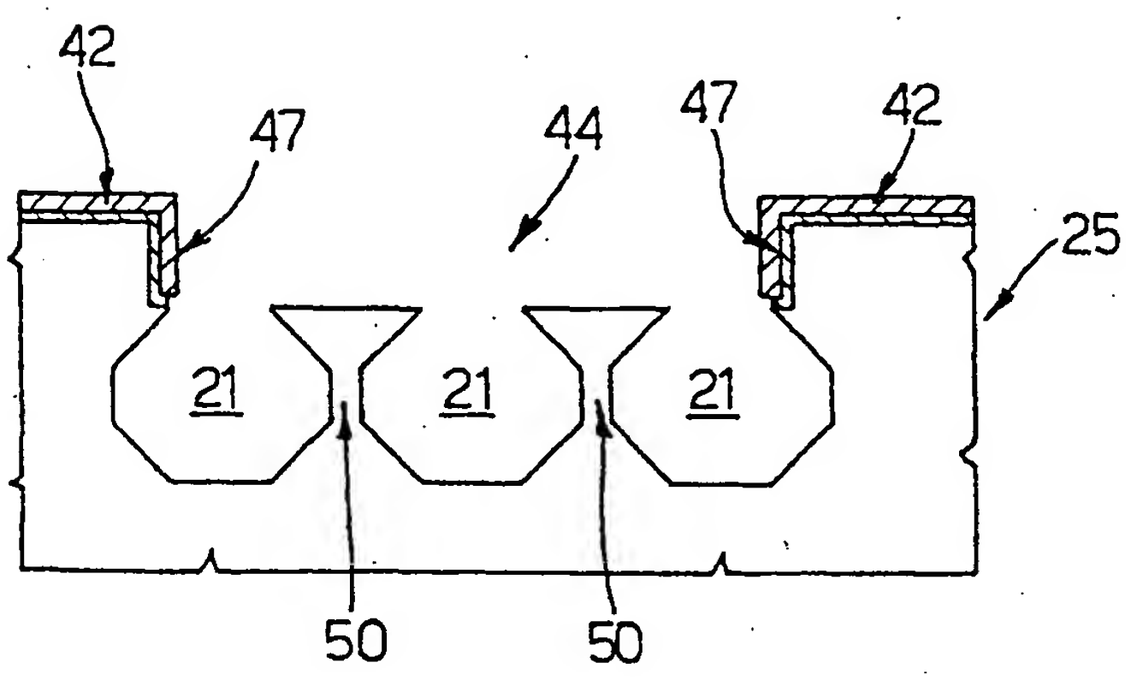


Fig. 26

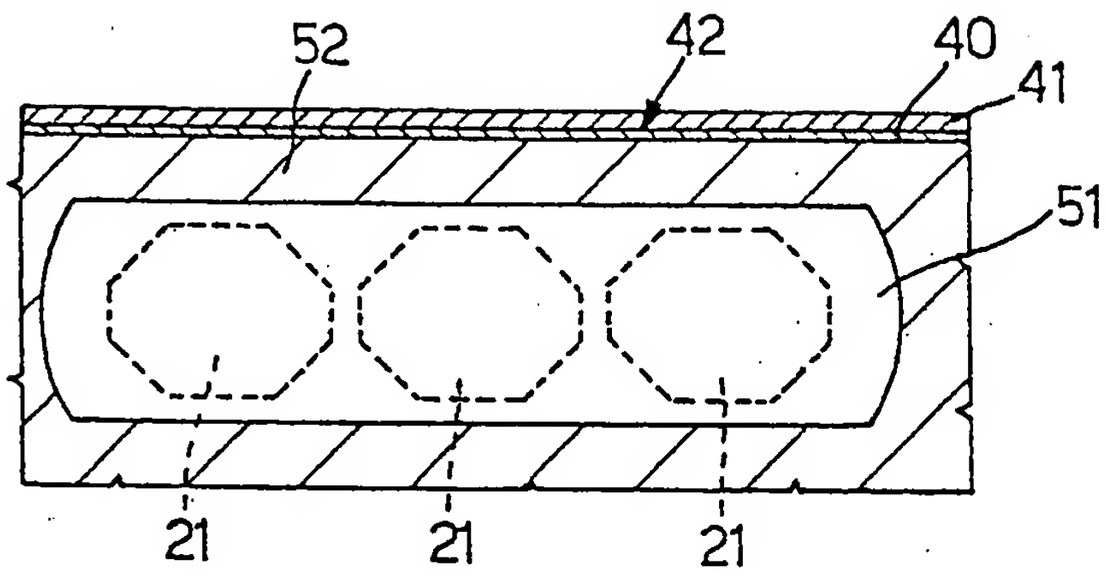


Fig. 27

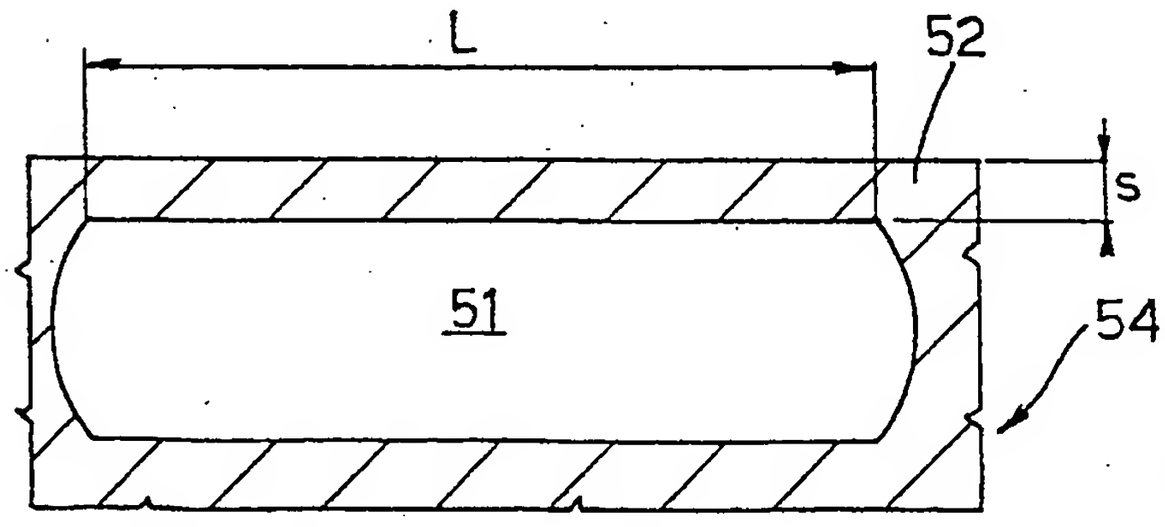


Fig. 28